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MULTI-GATE HETEROSTRUCTURED FIELD EFFECT TRANSISTOR

RELATED APPLICATION

This application claims the benefit of U.S. Provisional Application No.
5 60/431,631, filed on December 5, 2002, the entire teachings of which are incorporated
herein by reference.

BACKGROUND

A large class of Heterostructured Field Effect Transistors (HFETs) includes
Modulation Doped Field Transistors (MODEFETs), High Electron Mobility Transistors
10 (HEMT), Two-Dimensional Electron Gas Field Effect Transistors (TEGFETs), and
Selectively Doped Heterostructure Transistors (SDHTs) among others. All of these have
a non-uniform heterostructure (interface) potential along a channel of a HFET. As in
the case with a non-uniform electrical field in conventional FETs, a non-uniformity of
this heterostructure potential limits the gain g_m and operational frequency f_t , increases the
15 level of noise, and has a significant impact on the non-linearity of the gain.

Recently, some have proposed Transistors with Tailored Field (TTF) that have
the ability to manipulate the electrical field in FETs using external biases, which have
led to an increased average velocity of the electrons, and, therefore, a shorter transit
time.

SUMMARY

A heterostructured field effect transistor has a multi-gate configuration, in which the gate voltages are individually biased to tailor the potential field. The multi-gate configuration can be a two-, three-, or four-gate configuration. The transconductance of the transistor can be substantially linear over a range of gate voltages.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

FIG. 1 is a cross-sectional view a semiconductor transistor.

FIG. 2 is a plot of transfer (I_d) and transconductance (g_m) curves for p-HEMT in tailored (non-shaded squares and triangles) and non-tailored field regimes (solid squares and triangles) of operation.

FIG. 3 is a plot of the I-V characteristics for p-HEMT in a non-tailored regime of operation.

FIG. 4 is a plot of the I-V characteristics for p-HEMT in tailored field regime of operation.

DETAILED DESCRIPTION OF THE INVENTION

A description of preferred embodiments of the invention follows.

Conventional heterostructure transistors like High Electron Mobility Transistor (HEMT) operate rather differently than metal semiconductor field effect transistor (MESFET). In HEMTs, the electrons are injected into an intrinsic layer of a semiconductor material and are confined into a two-dimensional space of a heterostructure potential ϕ . At a given temperature, the mobility of the injected

electrons is the highest along the intrinsic layer, which improves power performance and increases the frequency of operation, f_t .

Quantization of electron energy in a two dimensional (2D) electron gas follows the equation:

$$E_n = \frac{\pi \hbar^2 n^2}{2m^* W^2} \quad (1)$$

where \hbar is the reduced Planck's constant, m^* is the effective mass of an electron, n is the quantum number, W is the width of the triangle heterostructure potential, or quantum well. The number of energy subbands E_n and their value define the distribution of electrons in the channel. Presence of discrete energy levels leads to reduction of noise, and may minimize hot electron damage, if subbands with high energy are not available in the 2D electron gas. This, however, is not realized in existing designs of HEMTs.

The energy and electron wave function can be defined from an equation such as

$$\sqrt{\frac{2m^*E}{\hbar^2}} \tan\left(\sqrt{\frac{2m^*E}{\hbar^2}} \frac{W}{2}\right) = \sqrt{\frac{2m^*(\phi(x)-E)}{\hbar^2}} \quad (2)$$

where E is the energy of the electron, and the heterostructure potential ϕ is provided by the equation:

$$\phi(x) = V_{bi} + V_D - V_G \quad (3)$$

Hence, with no drain bias V_D the heterostructure potential ϕ is equal to the built-in potential V_{bi} plus the gate bias V_G , and the potential ϕ is uniform in height and shape along the channel. Thus, when $V_G = 0$, $\phi = V_{bi}$, so that basic energy subbands are

present. But with applied gate and drain biases, V_G and V_D , the potential $\phi(x) = f(V_G, V_D)$ becomes a complicated, non-uniform function of the terminal voltages.

The drawbacks of HEMTs are well known. Like MESFETs, electrons in HEMTs move slowly from the source along a substantial portion of a channel, while any applied biases change the width of the quantum well since the width is a function of the drain and gate biases, i.e. $W = f(V_G, V_D)$. Such applied biases modify the spectra of energy subbands along the channel. Although the transcendental equation (2) is typically solved by numerical methods, a simple assessment shows that at the source side, where $\phi(x) = V_{bi} + V_G$, the respective subbands for $n = 1, 2, 3$ are

$$E_1 = 0.015 \text{ eV}$$

$$E_2 = 0.06 \text{ eV}$$

$$E_3 = 0.15 \text{ eV}$$

However, E_3 does not actually exist because $E_3 > q\phi$, where q is the electron charge.

At the drain side, where, for example, $V_D = 6\text{V}$ to 8V , the subbands for $n = 1, 2, 3$ are

$$E_1 = 1.5 \text{ eV}$$

$$E_2 = 6 \text{ eV}$$

$$E_3 = 13 \text{ eV}$$

and $E_4 > q\phi$.

As a cluster of electrons moves along the channel, the energy distribution of the electrons occurs, causing noise phenomena and hot electron damage. However, in the case of tailoring, the population of energy levels in the 2D electron gas is the same. Electrons moving through the channel will face decreased impurity scattering because of the intrinsic nature of the material, but they will still face phonon scattering. However, based on the calculations described above, the electron energies (energy levels) will vary along the channel, generating noise.

At operation frequencies, f_p , of about 5GHz, hot electron damage typical occurs, and the noise level is about 2 dB for certain performers in the class of heterostructure devices.

Contrary to existing HEMT designs, here, a multi-gate (two, three, and four gates) HFET configuration is used, where a more uniform potential field $\phi(x)$ is created by balancing the gate voltages. Tailoring of the potential along the channel of HEMT creates uniform distribution of energy subbands. The uniform potential accelerates the electrons as they are injected into the channel. As a result, the average electron velocity, as well as the frequency of operation f_t , increases. The values of the energy subbands are limited and are about the same along the channel, thereby minimizing noise and hot electron damage.

Although dual-gate HEMTs are known, these are mostly used for cascade circuits, i.e. using two transistors in one, but not for tailoring the heterostructure potential.

In the illustrated embodiment, transistors with the special trapezoidal gate design are used, such as the gates 12 shown in FIG. 1. The trapezoidal shape of the gates and the top metalization allows placing two submicron gates very close together, which improves the efficiency of tailoring.

In the various embodiments, the heterostructure transistors are manufactured with two, three, and four gates. The tailored tri-gate embodiment 10 is fabricated on M/A-COM's high volume production AlGaAs/InGaAs process. AuGe/Ni/Au ohmic contacts 14 are formed in a heavily-doped GaAs cap layer 16. Gates 12 that are 0.5 μm in length are optically patterned and realized with a Ti/Pt/Au metal lift-off process in a double recessed channel. Interconnects 17 are positioned over respective contacts 14, and the entire die is covered with a Si_3N_4 passivation layer 18. In the present invention, the gates 12 are individually biased with a respective potential, while in a conventional design the gates 12 are connected together such that the same potential is applied to all three gates.

Referring now to FIGs. 2-4, there is shown a comparison of the I-V characteristics of a tailored tri-gate structure with a conventional tri-gate design. The bias of the gates in the tri-gate structure is provided in a manner that makes the heterostructure potential uniform. The variation of electron energies are minimized by

making the width of the heterostructure barrier more uniform along the channel. This is accomplished by tailoring the field, that is, by making the slope of the 2D electron gas barrier more uniform along the channel. This allows the electrons to be energetic at the source, while not exceeding the energies that cause hot electron damage.

5 The I-V characteristics of a tri-gate HEMT for a case when three gates are connected together, i.e. non-tailored, are shown in FIG. 3, emulating the operation of a single gate conventional HEMT as well as a tri-gate switch. FIG. 3 shows the drain current versus drain voltage, V_D , for various gate biases or voltages, V_G . As can be seen, the spacing between the I-V curves changes. Accordingly, the transconductance
10 (g_m) is non-linear as shown by the plot of the solid squares in FIG. 2.

On the other hand, the spacing between the I-V curves is the same for a tri-gate p-HEMT for a case when three gates are biased separately, i.e. tailored, as shown in FIG. 4. In which case, the transconductance (g_m) is linear as shown by the non-shaded squares in FIG. 2. Thus, this direct comparison shows that the transconductance of a
15 HEMT with tailored fields is more linear than one for a conventional HEMT.

The versatility of the field tailoring is such that for a given particular specification the transistor performance can be improved. For example, if the gate biases are extended to positive voltages, the p-HEMT with the tailored field significantly outperforms the transistor operating in the conventional regime. Evidence
20 of this is shown in FIG. 2, which illustrates that the transfer curve, or the drain current I_d , of the p-HEMT with a tailored field (non-shaded triangles) is more linear than a p-HEMT with three gates connected together (solid triangles). For a non-tailored transistor, as soon as gate leakage current reaches unacceptable levels, from the readability point of view, the level of the transfer curve, I_d (solid triangles), as well as
25 the transconductance curve, g_m (solid squares), is cut off. For the transistor operating in the tailored mode, however, the critical gate leakage current is never reached, and the transconductance curve (non-shaded squares) and the transfer curve (non-shaded triangles) extend to a larger gate voltage range than the non-tailored device.

While this invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.